REMARKS

Claims 40, 43-46, 71, and 74-75 have been amended. Claims 76-86 have been added. Claims 40, 43-51, 68-72, and 74-86 are now pending. Applicant reserves the right to pursue the original claims and other claims in this and other applications. Applicant respectfully requests reconsideration of the above-referenced application in light of the amendments and following remarks.

Claims 40, 43-49, 69, 71-72 and 74-75 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Yamamoto in view of Svetkoff. The rejection is respectfully traversed.

The Examiner's Answer states that Yamamoto discloses a "solder contact/ball (48 in Fig. 7) formed in the second insulator layer." (pg. 4). Applicant respectfully disagrees. Yamamoto discloses a structure consisting of three insulating layers in FIG. 7: layers 24, 41, and 47. The first insulating layer 24 is formed over a portion of first connection electrode 23. The second insulating layer 41 is formed on top of first insulating layer 23. The third insulating layer is formed on surface active layers 43, 44 and second insulating layer 41. Yamamoto's solder bump 48 is formed only in third insulating layer 47. Yamamoto does not disclose "at least one solder contact formed in the second insulator layer," as recited in claim 40, or "at least one solder contact formed in the second insulating layer," as recited in claim 71.

The Examiner's Answer asserts that Yamamoto discloses "a second insulator layer (47 in Fig. 7) overlying the metal pad." (pg. 4). Applicant respectfully disagrees. Layer 47 is not a second insulating layer but a third insulating layer. In FIG. 7, layer 41 is the second insulating layer and layer 24 is the first insulating layer. Since layer 41 is the second insulating layer, Yamamoto does not disclose "a second insulator overlying said at least one metal pad," as recited in claim 40, or "a second insulating layer formed

over said at least one metal pad," as recited in claim 71. Yamamoto teaches that second connection electrode 45 and interconnect 50 are formed on top of second insulating layer 41.

The Examiner's Answer further asserts that Yamamoto discloses a "metal pad . . . comprising a stack of three different metals/levels including zinc, or nickel, copper and gold (see 46a, 46b, and 50 in Fig. 4 and 7)." (pg. 4). Applicant respectfully disagrees. Yamamoto teaches that "through electroless plating of zinc, nickel, etc . . . a first conductive layer 46a for adhesive bond is thinly formed." (Col. 5, lines 13-15). Then, "through the electroless plating of copper . . . a second conductive layer 46b is formed on the first conductive layer 46a." (Col. 5, lines 18-20).

Yamamoto does not disclose or suggest the composition of interconnect line 50. Yamamoto merely discloses two layers: first conductive layer 46a and second conductive layer 46b. Yamamoto does not teach or suggest that the "metal levels comprise Zirconium, Nickel, Copper, and Gold," as recited in dependent claim 70, or that the "metal pad comprises a metal stack comprising four different metal levels," as recited in dependent claim 69. At most, Yamamoto discloses a metal stack comprising two metal levels: layer 46a and layer 46b.

Accordingly, Yamamoto does not teach or suggest a semiconductor device comprising "a semiconductor structure having at least one metal contact . . . a first insulator layer overlying said at least one metal contact; at least one metal pad overlying said first insulator layer . . . a second insulator layer overlying said at least one metal pad; and, at least one solder contact formed in the second insulator layer . . . having a diameter less than 100 microns," as recited in claim 40.

Similarly, Yamamoto does not disclose or suggest a semiconductor device having at least one metal contact formed thereon comprising "a first insulating layer formed over said at least one metal contact; at least one metal pad formed over said first insulating layer; a second insulating layer formed over said at least one metal pad; and at least one solder contact formed in the second insulating layer and in contact with said at least one metal pad, wherein said at least one solder contact has a diameter between 2 and 100 microns," as recited in claim 71.

The Examiner's Answer acknowledges that Yamamoto "fails to teach the diameter of the solder contact being less than 100 microns." (pg. 5). Svetkoff is relied upon for disclosing a miniature/micro ball grid array device using solder balls having a typical range of 10-300 microns. Applicant respectfully submits, however, that there is no motivation to combine the references, that combining the references would require substantial reconstruction and redesign of the elements, and that the references are non-analogous art and thus, one skilled in the art would not have combined them.

The Examiner's Answer states that it would be obvious to combine Svetkoff with Yamamoto "so that interconnect density can be improved and the device size/ground rules can be reduced in Yamamoto's device." (pg. 5). Applicant respectfully directs the Examiner's attention, however, to Yamamoto col. 6, lines 1-8 and FIG. 6, where Yamamoto teaches that "[a]ccording to the semiconductor device structure of the present embodiment, since those solder bumps 48 on the second connection electrodes are arranged as a matrix array . . . it is possible to make the pitch BP between the mutually adjacent solder bumps 48 very larger [sic]."

Thus, in FIG. 6, Yamamoto's structure allows solder bumps 48 to be spaced apart further away from other solder bumps. Yamamoto teaches away from increasing the interconnect density. Consequently, there is no motivation to combine Svetkoff,

which creates a higher interconnect density through a larger number of solder balls, as alleged by the Office Action, with Yamamoto, which discloses spacing the solder balls farther apart, thereby decreasing interconnect density. Moreover, Svetkoff is directed to an imaging patent. Neither Yamamoto nor Svetkoff discloses a solder ball array structure or its method of formation.

Applicant respectfully submits that even if Yamamoto and Svetkoff are properly combinable, which they are not, the combination results in substantial reconstruction and redesign of the elements. It is not proper to combine references where doing so "would require a substantial reconstruction and redesign of the elements shown in [the primary reference, i.e., Yamamoto] as well as a change in the basic principle under which the [primary reference, i.e., Yamamoto] construction was designed to operate." In re Ratti, 270 F.2d 810, 813, 123 U.S.P.Q. 349, 352 (C.C.P.A. 1959). This is well settled Office policy. See M.P.E.P. § 2143.01, page 2100-127 (Feb. 2003).

The "modification" proposed by the Examiner, in the rejection of claims 40, 43-49, 69, 71-72 and 74-75, would require a substantial reconstruction and redesign of the elements of the Yamamoto semiconductor structure as well as a change in the basic principle under which it was designed to operate (forming a thinner and more reliable structure). Yamamoto is directed to a semiconductor device where "no sub-printed circuit board is used . . . so that a whole device structure can be made thinner . . . [and] since no elastic bonding layer 15 is used . . . there arises almost no connection position displacement . . . during a thermal pressure bonding . . . and obviate[s] the need to make bond checking." (Col. 6, lines 9-26). Thus, Yamamoto can form solder balls at a farther distance apart to make the pitch BP between "mutually adjacent solder bumps 48 very larger [sic]." (Col. 6, line 9). The proposed modification to Yamamoto would not allow the pitch BP between solder bumps 48 to be large. A major reconstruction

and redesign would be required.

Moreover, Applicant respectfully submits that Yamamoto and Svetkoff are non-analogous art. A reference is "reasonably pertinent" if, "even though it may be in a different field from that of the inventor's endeavor, it is one which, because of the matter with which it deals, logically would have commended itself to an inventor's attention in considering his problem." In re Clay, 966 F.2d 656, 659 (Fed. Cir. 1992).

Svetkoff describes a system and method for "three-dimensional imaging of 'non-cooperative' targets that are typically difficult to measure by optical means due to light reflection, scattering and geometry." (Col. 1, lines 59-61; col. 5, lines 2-5). The Svetkoff imaging system is not analogous to the semiconductor device of the present invention.

"In order to rely on a reference as a basis for rejection of an applicant's invention, the reference must either be in the field of applicant's endeavor or, if not, then be reasonably pertinent to the particular problem with which the inventor was concerned." In re Oetiker, 977 F.2d 1443, 1446 (Fed. Cir. 1992); M.P.E.P. § 2141.01(a). A reference is "reasonably pertinent" if, "even though it may be in a different field from that of the inventor's endeavor, it is one which, because of the matter with which it deals, logically would have commended itself to an inventor's attention in considering his problem." In re Clay, 966 F.2d 656, 659 (Fed. Cir. 1992).

Svetkoff does not relate to the field of the present invention, e.g., A micro solder ball for use in a C4 bonding process, and this fact is illustrated by the accompanying text. As stated in Svetkoff, "[r]eferring specifically to Fig. 5, an object of the invention is to provide a high speed method and system for measuring a miniature spherical mirror like a solder ball 46 or wafer, mounted on a plane mirror or pad 48

formed on a substrate 50 and producing a very high contrast bump-background image allowing for accurate measurement of diameter, devoid of occlusion and with minimal reflection noise for many pad backgrounds. Fig. 5 shows a spatial filter 52 through which an incident ray 54 passes and bounces off the ball surface to form reflected rays 56, multiple reflections 58, and specular reflection 60. The spatial filter 52 (i.e. confocal slit) provides the indicated filtering action." (Col. 6, lines 25-37).

Svetkoff's disclosure indicates that it is clearly different from Applicant's field of endeavor. Significantly, Svetkoff does not teach or suggest how to make a semiconductor device with solder balls. Svetkoff's solder balls are not part of the invention therein and are simply given as an example of the size of non-cooperative targets that may be studied by the claimed invention. In other words, Svetkoff does not teach a die having solder balls in Applicant's claimed diameter range of 2-300 microns. Svetkoff merely discloses that the disclosed optical system is capable of studying solder balls in that range. There is nothing in Svetkoff to teach or suggest how to make or use a die having solder balls in the range of 2-300 microns. The Examiner's answer has already conceded that Yamamoto does not teach or suggest a solder ball or method of making it.

Since Svetkoff is directed to an imaging system and has no disclosure of how to make a semiconductor device, much less one having solder balls less than 100 microns in diameter, it cannot permissibly be combined with the teachings of Yamamoto to render the claimed invention obvious. The two fields (Yamamoto's semiconductor device and Svetkoff's imaging device) involve entirely distinct problems and solutions. Therefore nothing commends looking at Svetkoff's field, to an inventor attempting to improve integrated circuit chip density. See M.P.E.P. § 2141.01(a). For at least the reasons provided above, Yamamoto and Svetkoff are not properly combinable.

Further, even if Svetkoff is analogous, which it is not, it still does not sufficiently teach how to make the imaged solder balls described therein. In other words, Svetkoff does not relate to solder contacts and does not include an enabling disclosure for making any solder contacts.

Even assuming arguendo that Svetkoff is directed to analogous prior art, which it is not, Svetkoff's disclosure with respect to solder balls is insufficient to teach one of ordinary skill in the art how to make a semiconductor device having solder balls less than 100 microns in diameter. As mentioned above, Svetkoff mentions that his system can image solder balls or bumps 10-300 microns in diameter (col. 11, line 27-37). However, this is merely a bald reference to an example of a microelectronic or micromechanical device which can be studied in Svetkoff, and not an enabling disclosure of a die structure having solder balls 2-300 microns in diameter. Indeed, there is absolutely no disclosure in Svetkoff for making a semiconductor device having solder balls in the disclosed range, and certainly no teaching for making a semiconductor device having solder balls less than the claimed 100 microns in diameter.

The Federal Circuit stated, "[i]n order to render a claimed apparatus or method obvious, the prior art must enable one skilled in the art to make and use the apparatus or method." Beckman Instruments, Inc. v. LKB Produkter AB, 892 F.2d 1547, 1551, 13 USPQ2d 1301, 1304 (Fed. Cir. 1989) (citing In re Payne, 606 F.2d 303, 314, 203 USPQ 245, 255 (CCPA 1979) ("References relied upon to support a rejection under 35 USC 103 must provide an enabling disclosure, i.e., they must place the claimed invention in the possession of the public. An invention is not 'possessed' absent some known or obvious way to make it.") (quoting In re Hoeksema, 399 F.2d 209, 274 (C.C.P.A. 1968)). The Federal Circuit reiterated this proposition in Motorola Inc. v. Interdigital Technology Corp., 121 F.3d 1461, 1472, 43 USPQ2d 1481, 1489 (Fed. Cir.

1997) (quoting Beckman, supra).

Where the reference does not include an enabling disclosure, "secondary evidence, such as other patents or publications, can be cited to show public possession of the method of making and/or using [the claimed article]." M.P.E.P. § 2121.01(I). Here, there is no such enabling disclosure as the Examiner's answer fails to cite any secondary evidence that a method of making and/or using solder balls less than 100 microns in diameter was in the public possession at the time of the present invention.

Claims 43-49, 69, and 74-75 depend from claim 40. Claim 72 depends from claim 71. Claims 43-49, 69, 72, and 74-75 should be allowable along with their base claims for at least the reasons provided above.

Moreover, the references fail to disclose or suggest "solder contacts [that] have a diameter less than 10 microns," as recited in claim 43. The references also fail to disclose or suggest "solder contacts [that] have a diameter of approximately 2 microns," as recited in claim 44, or that "at least one solder contact has a diameter of approximately 2 microns," as recited in claim 71. Svetkoff is relied upon for disclosing solder balls that are 10 to 300 microns in diameter. A solder ball formed to less than 10 microns in diameter would not be rendered obvious by Yamamoto and Svetkoff, much less a solder ball that is approximately 2 microns in diameter.

The references also fail to teach or suggest that the "first insulator layer is at least 2 microns thicker than said at least one metal contact," as recited in claim 68. The Examiner's Answer asserts that Yamamoto discloses a "first insulating layer being 10-50 microns thick (41 in Fig. 7)." (pg. 7). Again, however, layer 41 is the second insulating layer in Yamamoto's chip 21. Layer 24 is the first insulating layer. Yamamoto does not even teach or suggest a thickness for first insulating layer 24.

These are additional reasons for the allowance of dependent claims 43, 44, 68, and 71.

Claims 50 and 51 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Yamamoto and Svetkoff and further in view of the admitted prior art. The rejection is respectfully traversed.

Claims 50 and 51 depend from claim 40 and are allowable for at least the reasons provided above regarding claim 40. In particular, Yamamoto and Svetkoff do not teach or suggest a second insulator layer overlying at least one metal pad or at least one solder contact formed in the second insulator layer having a diameter less than 100 microns. Moreover, since Yamamoto discloses forming solder bumps 48 that are spatially separated farther apart, there is no motivation to use the solder bumps of Svetkoff.

Claim 69 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Yamamoto and Svetkoff and further in view of Wojnarowski. The rejection is respectfully traversed.

Claim 69 depends from claim 40 and should be allowable for at least the reasons provided above regarding claim 40. Wojnarowski is relied upon for disclosing a pad metallization comprising four or more layers, and adds nothing to rectify the deficiencies of Yamamoto and Svetkoff. In particular, Yamamoto and Svetkoff do not teach or suggest a second insulator layer overlying at least one metal pad or at least one solder contact formed in the second insulator layer having a diameter less than 100 microns. Moreover, since Yamamoto discloses forming solder bumps 48 that are spatially separated farther apart, there is no motivation to use the solder bumps of Svetkoff which would decrease the spatial distance between Yamamoto's solder bumps.

Moreover, there is no motivation to combine Wojnarowski with Yamamoto. As indicated previously, Yamamoto is directed to forming a thinner semiconductor structure. Wojnarowski's additional metal layers would increase the size of Yamamoto's structure. This would defeat the very problem that Yamamoto is directed to solving: forming a thinner semiconductor device. This is an additional reason for the allowance of claim 69.

Claim 70 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Yamamoto and Svetkoff and Wojnarowski, and further in view of Takashi. The rejection is respectfully traversed.

Claim 70 depends from claim 69 which depends from claim 40. Claim 70 should be allowable for at least the reasons provided above regarding claim 40 and 69. Takashi is relied upon for disclosing a metal pad comprising Zirconium, and adds nothing to rectify the deficiencies of Yamamoto, Svetkoff, and Wojnarowski.

In particular, the cited references do not teach or suggest a second insulator layer overlying at least one metal pad or at least one solder contact formed in the second insulator layer having a diameter less than 100 microns. Further, since Yamamoto discloses forming solder bumps 48 that are spatially separated farther apart, there is no motivation to use the solder bumps of Svetkoff which would decrease the spatial distance between Yamamoto's solder bumps. Further still, there is no motivation to combine Yamamoto and Wojnarowski since they teach away from each other. Yamamoto discloses forming a thinner structure while Wojnarowski discloses additional metal pad layers, thus, forming a thicker structure.

Applicant also respectfully submits that the prior art of record neither teaches nor discloses a semiconductor device comprising, "a semiconductor structure having at

least one metal layer formed over a surface thereof; a first insulating layer formed over said at least one metal layer, wherein said first insulating layer is at least two microns thicker than said at least one metal layer; at least one metal stack formed over said first insulating layer and in contact with said at least one metal layer; a second insulating layer formed over said at least one metal stack; and, an etched solder layer having a thickness of at least 2.33 microns, wherein said etched solder layer forms at least one solder contact in said second insulating layer and in contact with said at least one metal stack," as recited in claim 76.

The prior art of record does not teach or suggest an etched solder layer having a thickness of at least 2.33 microns. Similarly, the prior art of record does not teach that the first insulating layer is at least two microns thicker than the metal layer. Claims 77-86 depend from claim 76 and should be similarly allowable along with claim 76.

In view of the above, claims 40, 43-51, 68-72, and 74-86, are believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to pass this application to issue.

Dated: October 25, 2004

Respectfully submitted,

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